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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,680	12/16/2003	Takahito Nakano	246575US6	3581

22850 7590 03/03/2006

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EXAMINER	
FRANKLIN, RICHARD B	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,680	NAKANO ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 8 have been examined.

Drawings

2. Figure 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Applicant is advised that should claim 1 be found allowable, claim 8 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). Claim 8 recites all the limitations of claim 1 except the storage means and output means of claim 1 have been claimed as a storage section and an output section respectively.

4. Claim 5 is objected to because of the following informalities:

a. As per claim 5, the statement "storage means for allowing reading out from and writing in to outside" is not clear or understandable in the context of the claim. The Examiner has taken the best reasonable interpretation of this limitation while examining the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada US Patent No. 6,889,299 (hereinafter Yamada).

As per claims 1 and 8, Yamada teaches a semiconductor integrated circuit apparatus mounted on a predetermined circuit board, the apparatus comprising: semiconductor information storage means for storing semiconductor information unique to the semiconductor integrated circuit apparatus (Figure 9 Item 61, Col 8 Lines 49 – 53); and semiconductor information output means connected to the semiconductor information storage means for reading out the semiconductor information from the semiconductor information storage means in response to a signal supplied from outside

and outputting the read-out semiconductor information to the outside (Figure 9 Item 62, Col 8 Lines 49 - 53).

As per claim 2, Yamada also teaches wherein the semiconductor information output means comprises connection control means (Figure 9 Item 62), which is to be connected to predetermined external storage means (Figure 9 Item 212), for controlling a write-in operation of information to the external storage means (Col 8 Lines 23 – 29), and control means for controlling the write-in operation to write the read-out semiconductor information into a predetermined region of the external storage means via the connection control means (Figure 9 Item 63, Col 8 Lines 23 – 29 and 58 – 63).

As per claim 3, Yamada also teaches wherein the semiconductor information output means comprises connection control means (Figure 5 Item , which is to be connected to predetermined external storage means (Figure 5 Item 202) storing a program (Figure 5 Item 201), for controlling a read-out operation of the program stored in the external storage means (Col 6 Lines 29 – 36), the program being used for executing the read-out operation of the semiconductor information (Col 6 Lines 29 – 36), and control means for controlling the read-out operation and external outputting operation of the semiconductor information based on the read-out program via the connection control means (Figure 5 Item 32, Col 6 Lines 29 – 36).

As per claim 4, Yamada also teaches wherein the semiconductor information storage means stores an identification code as the semiconductor information (Figure 1 Item 61), the identification code being assigned to allow identification of the semiconductor integrated circuit apparatus, and outputs an electric signal according to the identification code in response to an input of a read-out signal (Col 8 Lines 49 – 53).

As per claim 5, Yamada teaches a circuit board on which a semiconductor integrated circuit apparatus is mounted, the circuit board comprising: storage means for allowing reading out from and writing into (Figure 9 Item 212, Col 8 Lines 53 – 55); semiconductor information storage means for storing semiconductor information unique to the semiconductor information circuit apparatus (Figure 9 Item 61, Col 8 Lines 49 – 53); and semiconductor information output means (Figure 9 Item 62), which is to be connected to the semiconductor information storage means, for reading out the semiconductor information from the semiconductor information storage means in response to a signal supplied from outside and writing the read-out semiconductor information into the storage means (Col 8 Lines 49 – 53).

As per claim 6, Yamada also teaches wherein the storage means stores a program (Figure 5 Item 201) being used for executing the read-out operation of the semiconductor information (Col 6 Lines 29 – 36), and wherein the semiconductor information output means controls the read-out operation of the semiconductor information based on the program read out from the storage means (Col 6 Lines 29 –

36), and the write-in operation of the semiconductor information to the storage means (Col 6 Lines 29 – 36).

As per claim 7, Yamada teaches an information readout method of reading out semiconductor information of a semiconductor integrated circuit apparatus, the method comprising the steps of: writing a program, which is for reading out semiconductor information unique to the semiconductor integrated circuit apparatus and stored in the semiconductor integrated circuit apparatus (Figure 5 Item 201), into a predetermined external storage means, reading the program written into the external storage means and reading out the semiconductor information based on the program (Col 6 Lines 29 – 36), and writing the read-out semiconductor information into a predetermined region of the external storage means (Col 6 Lines 29 – 36).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard Franklin
Patent Examiner
Art Unit 2181

KIM HUYNH
SUPERVISORY PATENT EXAMINER

2/25/06